SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Applications No. 2011-128604 filed on Jun. 8, 2011; 2011-142148 filed on Jun. 27, 2011; and 2012-111746 filed on May 15, 2012, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to a semiconductor device and a manufacturing method thereof. The semiconductor device includes a region for isolating an active region in which a transistor having a trench gate structure is formed, and a marginal region which surrounds the outer periphery of the active region and defines an outer edge of the semiconductor device.

BACKGROUND

[0003] In order to prevent mutual interference of a plurality of elements formed on a semiconductor substrate, there is conventionally known technology in which the elements adjoining each other are electrically isolated.

[0004] For example, there is known a method that includes a step of sequentially layering a silicon oxide film and a silicon nitride film on a silicon substrate and removing a portion of the silicon nitride film by etching using a photoresist as a mask, a step of selectively oxidizing a portion of the silicon oxide film exposed by the removal of the silicon nitride film to thereby form a LOCOS oxide film in the exposed portion of the silicon oxide film, and a step of forming buried oxide films on the silicon substrate at opposite sides of the LOCOS oxide film. In this method, an inter-element isolating region is made up of the LOCOS oxide film and the buried oxide films.

[0005] The above-described element isolating technology may also be used in, for example, electrically isolating an active region in which an element is formed from a marginal area defining an outer edge of a semiconductor device.

SUMMARY

[0006] A semiconductor device of the present disclosure includes: a first-conductivity-type semiconductor layer including an active region in which a transistor having a plurality of impurity regions is formed and a marginal region surrounding an outer periphery of the active region; a second-conductivity-type channel layer formed between the active region and the marginal region so as to form a front surface of the semiconductor layer; at least one gate trench formed in the active region to extend from the front surface of the semiconductor layer through the channel layer; a gate insulation film formed on an inner surface of the at least one gate trench; a gate electrode formed inside the gate insulation film in the at least one gate trench; and at least one isolation trench arranged between the active region and the marginal region to surround the outer periphery of the active region and formed to extend from the front surface of the semiconductor layer through the channel layer, the at least one isolation trench having a depth equal to a depth of the at least one gate trench.

[0007] With this configuration, the channel layer extending between the active region and the marginal region is partitioned by the at least one isolation trench, thereby providing insulation and isolation between the active region and the marginal region. Accordingly, the channel layer of the active region can be electrically isolated from the channel layer of the marginal region.

[0008] While a method of electrically isolating the channel layer of an active region is conventionally available, the conventional method differs from the method of the present disclosure in which isolation trenches are formed in the semiconductor device. The conventional method suffers from a number of problems.

[0009] Specifically, in the conventional method, ion implantation for forming the channel layer is performed after a LOCOS oxide film in the surface layer portion of the semiconductor layer or a recess LOCOS oxide film is formed by thermal oxidation. Therefore, even if ions are accelerated toward the entire area of the front surface of the semiconductor layer, the accelerated ions are blocked by the LOCOS oxide film in the surface layer portion or the recess LOCOS oxide film. Thus, implantation of the ions toward the portions directly below the LOCOS oxide film in the surface layer portion or the recess LOCOS oxide film is prevented. Accordingly, the channel layers are separately formed at the side of the active region and the side of the marginal region with respect to the LOCOS oxide film enabling the channel layer of the active region to be electrically isolated from the channel layer of the marginal region.

[0010] However, in the conventional method, the LOCOS oxide film needs to be formed relatively thick in order to adjust the electric fields generated from the terminal of the transistor. For this reason, it is necessary to perform the heat treatment for a long period of time when forming the LOCOS oxide film, which may result in deterioration of the device characteristics of the semiconductor device. Further, if the width of the LOCOS oxide film (the element isolation width) is too small, the active region and the marginal region cannot be appropriately isolated. For this reason, a wide area is required for element isolation, which may result in a problem in that the size of the semiconductor device grows larger.

[0011] In contrast, with the semiconductor device of the present disclosure, the active region and the marginal region are electrically insulated and isolated from each other by the at least one isolation trench. Therefore, even if the width of the at least one isolation trench is smaller than the width of the LOCOS oxide film, the channel layers can be completely divided. Accordingly, the size of the semiconductor device can be reduced.

[0012] The semiconductor device of the present disclosure can be manufactured by a manufacturing method of a semiconductor device, which includes: forming a hard mask on a first-conductivity-type semiconductor layer having an active region and a marginal region surrounding an outer periphery of the active region; simultaneously forming at least one gate trench in the active region and at least one isolation trench surrounding the outer periphery of the active region between the active region and the marginal region, by selectively etching the semiconductor layer from a front surface thereof using the hard mask; forming a channel layer extending between the active region and the marginal region and divided by the at least one isolation trench between the active region and the marginal region, by implanting a second-conductivity-type impurity into a surface layer portion of the semiconductor layer while keeping an entire area of the front surface of the semiconductor layer exposed; forming a gate insulation film